life.augmented

ST4E1216, ST4E1240

Datasheet

High-speed 3.3 V / 5 V RS485 transceiver with ±12 kV IEC 61000-4-2 contact ESD protection

SO8 (4.90 x 3.91 mm)

DFN8 (3 x 3 mm)

Maturity status link
ST4E1216, ST4E1240

Device summary			
Part number	Data rate (Mbps)	Package	Temperature range
ST4E1240DT	40	SO8	-40°C; 85°C
ST4E1240IQT	40	DFN8	-40°C; 125°C
ST4E1216IDT	16	SO8	-40°C; 125°C

Features

- Meets or exceeds TIA/EIA-485A standard requirements
- 3 V to 5.5 V supply voltage
- Differential output voltage (V_{OD}) exceeds 2.1 V at 5 V supply for PROFIBUS compatibility
- High speed: up to 40 Mbps data rate
- More than 64 transceivers on the bus (up to 100 nodes)
- Integrated protections
  - Fail-safe receiver (bus open, idle, and shorted)
  - Thermal shutdown protection
  - Hot-swap capability (with parasitic capacitance up to 100 pF)
  - Bus I/O ESD protection
    - ±12 kV IEC61000-4-2 contact discharge
    - ±30 kV HBM
    - ±4 kV IEC61000-4-4 class-A fast transient burst (EFT)
- Low quiescent current in shutdown mode
- Available in industry standard SO-8 and DFN8 for the ST4E1240

Applications

- Factory automation and control
- Motion controllers
- Building automation and safety
- Video surveillance (building, traffic monitoring)
- Backplane busses
- Grid infrastructure
- Data acquisition (smart meters, seismic networks)

Description

The ST4E1216 and ST4E1240 are low-power differential line transceivers for data transmission standard RS485 applications in half-duplex mode, compatible with either 3.3 V or 5 V rail power supplies, fully operating from 3 V to 5.5 V.

The ST4E1216 and the ST4E1240 operate respectively up to 16 Mbps and 40 Mbps. They are ideal for multipoint applications over extended cable runs. They are robust to ESD transients. In particular, the bus pins support ±12 kV IEC 61000-4-2 contact discharge. They also feature robust hot-swap capability during switching on and off, or during hot insertion.

The ST4E1216 is available in SO8 and up to 125 °C. The ST4E1240 is available in SO8 and DFN8 with two temperature ranges as stated in the device summary table.

1 Pin configuration

Figure 1. Pin connections

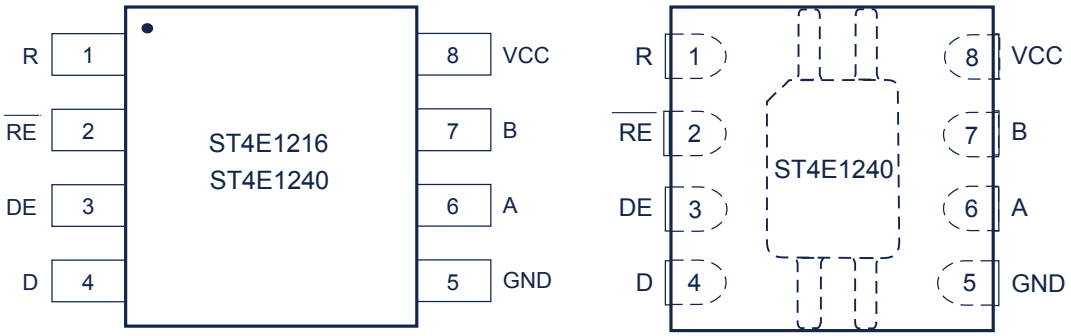


Table 1. Pin description

Name	Pin	I/O	Description
R	1	Digital output	Receiver data output
$\overline{RE}$	2	Digital input	Receiver enable input, active low
DE	3	Digital input	Driver enable input, active high
D	4	Digital input	Transmission data input
GND	5	Ground	
A	6	Bus I/O	Digital bus I/O, A
B	7	Bus I/O	Digital bus I/O, B
VCC	8	Device supply	3 V to 5.5 V supply voltage
EP		Exposed pad	DFN8 only. Connect the exposed pad to ground for optimum thermal behavior.

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Device supply voltage	-0.5	7	V
	Voltage range at A or B inputs	-9	14	V
	Input voltage range at any logic pin (referred to an operating V_{CC})	-0.3	V_{CC} + 0.3	V
	Short-circuit duration (R, A, B) to GND	Continuous		
T_{stg}	Storage temperature	-65	150	°C

Note: All voltage values, except the differential voltage, are with respect to network ground terminal.

Table 3. ESD ratings

Symbol	Parameter	Value	Unit
ESD	IEC61000-4-2 ESD (contact discharge), bus terminals A, B	± 12	kV
	IEC61000-4-4 EFT (fast transient or burst) bus terminals A, B	± 4 (class A)	kV
	HBM compliance, bus terminals (A, B) and GND	± 30 (1) (2)	kV
	JEDEC standard 22, test method A114, HBM (Human Body Model), all other terminals	± 2	kV
	JEDEC standard 22, test method C101, CDM (Charged Device Model), all pins	± 1	kV

1. *JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.*
2. *JEDEC standard 22, test method A114, HBM (Human Boby Model), bus terminals (A, B), ≥ ±8 kV (limited by industrial tester capability).*

   Measurement for 20 A peak, 100 ns Transmission-Line Pulse (TLP), package level at room temperature.

3 Electrical characteristics

Table 4. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Device supply voltage	3		5.5	V
V_I	Input level at any bus terminal (separated or common-mode)	-7		12	V
V_{ID}	Differential input voltage	-7		12	V
I_O	Output current/driver	-70		70	mA
	Output current/receiver	-70		70	
R_L	Differential load resistance	54	60		Ω
C_L	Differential load capacitance		50		pF
D_R	Signaling rate for ST4E1216			16	Mbps
	Signaling rate for ST4E1240			40	
T_A	Operating free-air temperature for ST4E1216	-40		125	°C
	Operating free-air temperature for ST4E1240 in SO8 package	-40		85	
	Operating free-air temperature for ST4E1240 in DFN8	-40		125	

Operation is specified for internal (junction temperature) up to 150 °C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shutdown circuit, which disables the driver outputs when the junction temperature reaches 165 °C.

Table 5. Thermal information

Symbol	Parameter	Min.	Typ.	Max.	Unit
$R_{th\text{-}ja}$	Thermal resistance, junction-to-ambient, SO8		125		°C/W
	Thermal resistance, junction-to-ambient, DFN8		45		

Table 6. Power dissipation

Symbol	Parameter	Test conditions	Typ.	Unit
P_D	ST4E1240 power dissipation, with driver and receiver enabled	Unterminated, R_L = 300 Ω, C_L = 50 pF	310	mW
	V_{CC} = 5.5 V, T = 85 °C, 50% duty cycle at 40 Mbps signaling rate	RS485-load: R_L = 54 Ω, C_L = 50 pF	370	mW
	ST4E1216 power dissipation, with driver and receiver enabled	Unterminated, R_L = 300 Ω, C_L = 50 pF	140	mW
	V_{CC} = 5.5 V, T = 125 °C, 50% duty cycle at 16 Mbps signaling rate	RS485-load: R_L = 54 Ω, C_L = 50 pF	220	mW

Table 7. Receiver: operating conditions (V_{CC} = +3.0 V to 5.5 V, T_A = Tmin to Tmax, unless otherwise specified. Typical values are at V_{CC} = 5 V and T = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Receiver/DC						
V_{TH+}	Positive-going input threshold voltage	-7 V ≤ V_{CM} ≤ 12 V		-100	-10	mV
V_{TH-}	Negative-going input threshold voltage	-7 V ≤ V_{CM} ≤ 12 V	-200	-130		
V_{HYS}	Receivers differential input voltage hysteresis			30		
V_{OH}	Receivers high-level output voltage	$\overline{RE}$ = GND, I_{OH} = - 2 mA, (VA-VB) > 200 mV	V_{CC}-0.2			V
V_{OL}	Receivers low-level output voltage	$\overline{RE}$ = GND, I_{OL} = 2 mA, (VA-VB) < -200 mV			0.2	
I_{OZ}	Receivers output high-impedance current	0 ≤ V_R ≤ V_{CC}, $\overline{RE}$ = V_{CC}	-1		1	µA
I_{OS}	Receivers outputs short-circuit current	0 ≤ V_R ≤ V_{CC}	-90		90	mA
R_{in}	Receivers input impedance	-7 V ≤ V_{incm} ≤ +12 V	24 (1)			kΩ
I_i	Receivers input current	V_I = 12 V		140	250	µA
	DE = GND, V_{CC} = GND or +5.5 V	V_I = -7 V	-250	-120		
Receiver/switching characteristics						
t_r, t_f	Receivers output rise/fall time	C_L = 15 pF	0.5	3	7.5	ns
t_{PHL}, t_{PLH}	Receivers propagation delay time		12	20	25	ns
$t_{SK(P)}$	Receivers pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$, ΔV_{in} = 1.5 V				2	ns
t_{PLZ}	Receivers disable time, from low	C_L = 15 pF with 1 kΩ		5	20	ns
t_{PHZ}	Receivers disable time, from high	C_L = 15 pF with 1 kΩ		5	30	ns
t_{PZH}	Receivers enable time to output high	Driver enabled C_L = 15 pF with 1 kΩ		8	30	ns
t_{PZL}	Receivers enable time to output low	Driver enabled C_L = 15 pF with 1 kΩ		5	20	ns
$t_{PZH(shdn)}$	Receivers enable time from shutdown to output high	Driver disabled C_L = 15 pF with 1 kΩ		5	30	ns
$t_{PZL(shdn)}$	Receivers enable time from shutdown to output low	Driver disabled C_L = 15 pF with 1 kΩ		8	20	ns

1. *Guaranteed by design simulation in temperature.*

Table 8. Driver: operating conditions (V_{CC} = +3.0 V to 5.5 V, T_A = Tmin to Tmax, unless otherwise specified. Typical values are at V_{CC} = 5 V and T = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC driver/DC						
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60 Ω/375 Ω (Figure 2), $V_{CC} \geq$ 4.5 V -7 V ≤ V_{CM} ≤ +12 V	2.1			V
		R_L = 60 Ω/375 Ω (Figure 2) -7 V ≤ V_{CM} ≤ +12 V	1.5	3.5		
		R_L = 54 Ω (Figure 3)	1.5			
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L = 54 Ω, C_L = 50 pF	-50		+50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27 Ω load resistors	1	2.7	3 (1)	V
ΔV_{OC}	Change in differential driver output common-mode voltage		-0.12	-0.02	0.12	V
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage			0.9		
V_{OH}	Single-ended driver output High	A or B output, I_A or I_B = -20 mA	V_{CC}-0.4			V
V_{OL}	Single-ended driver output Low	A or B output, I_A or I_B = 20 mA			0.95	V
Driver/switching characteristics						
t_r, t_f	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF	0.5	5	7.5	ns
t_{PHL}, t_{PLH}	Driver propagation delay		4	8	20	
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL}–t_{PLH}\|$				3	
t_{PLZ}, t_{PHZ}	Driver disable time			11	20	
t_{PZL}, t_{PZH}	Driver enable time	Receiver enabled		7	20	
		Receiver disabled		7	20	

1. *For V_{CC} = 5.5 V and T < 0 °C, $V_{OC(SS)}$ max = 3.15 V.*

Table 9. Input logic interface (D, DE, $\overline{RE}$): (V_{CC} = +3.0 V to 5.5 V, T_A = Tmin to Tmax, unless otherwise specified. Typical values are at V_{CC} = 5 V and T = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
I_{In}	Input current	3 V ≤ V_{CC} ≤ 5.5 V, V_{in} = 0 or V_{CC}	-5		5	µA
	Input impedance on first transition (DE, $\overline{RE}$)			6		kΩ

Table 10. Supply current and protections: (V_{CC}= +3.0 V to 5.5 V, T_A = Tmin to Tmax, unless otherwise specified. Typical values are at V_{CC} = 5 V and T = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current						
I_{CC}	Supply current (quiescent)	Driver and receiver enabled DE = V_{CC}, $\overline{RE}$ = GND, no load		1.77	2.5	mA
		Driver enabled, receiver disabled DE = V_{CC}, $\overline{RE}$ = V_{CC}, no load		1	1.8	mA
		Driver disabled, receiver enabled DE = GND, $\overline{RE}$ = GND, no load		1	1.8	mA
		Driver and receiver disabled (shutdown mode) DE = GND, $\overline{RE}$ = V_{CC}, no load		0.6	3.5	µA
T_{TSD}	Thermal shutdown threshold			165		°C
T_{TSD_HYS}	Thermal shutdown hysteresis			13		
I_{OS}	Driver short-circuit output current	-7 V < V_{SHORT} < +12 V	-250		250	mA

4 Test circuits

In the schematics below, C_L includes fixture and instrumentation capacitance.

Figure 2. Driver differential output voltage with common-mode load

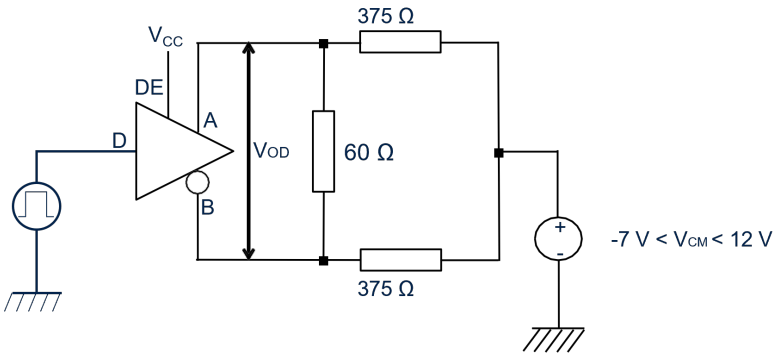


Figure 3. Driver differential and common-mode output with RS-485 load

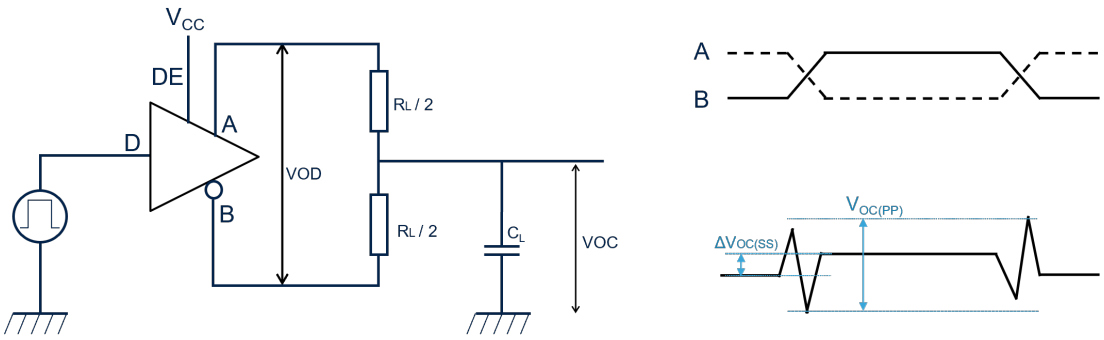


Figure 4. Driver differential output rise and fall times and propagation delays

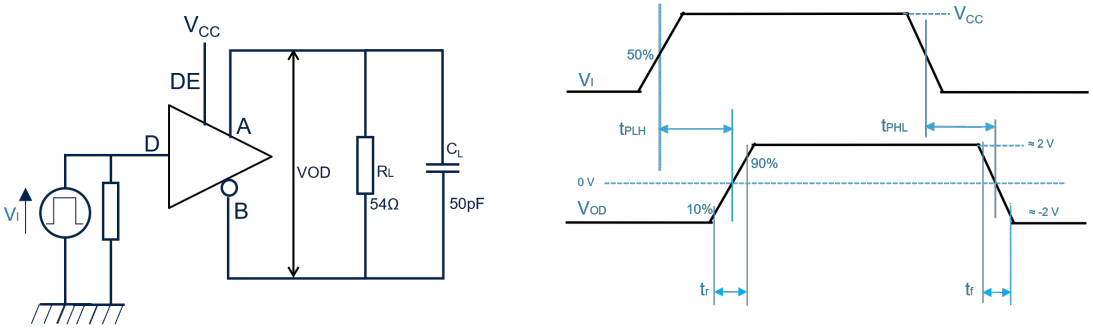


Figure 5. Driver enable and disable times with active high output and pull-down load

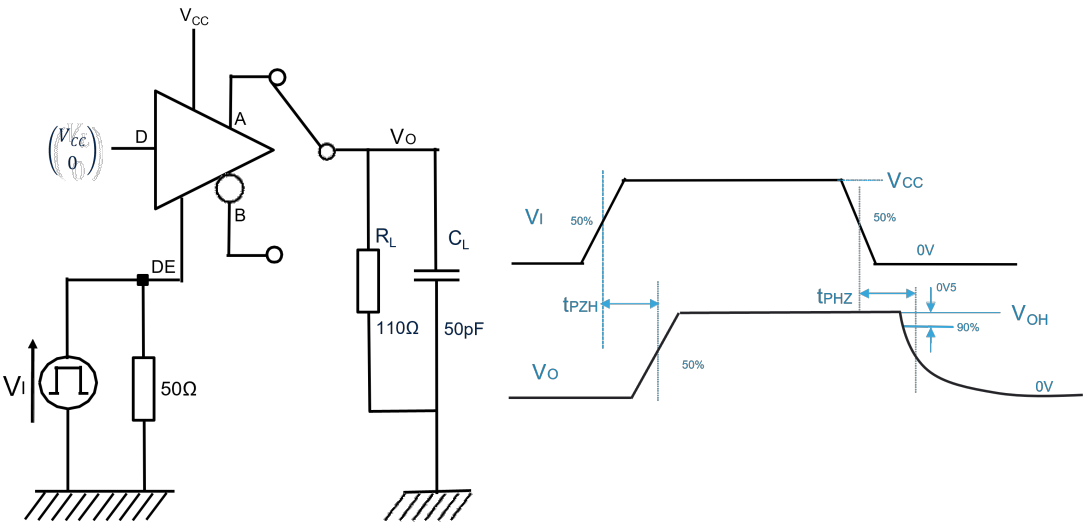


Figure 6. Driver enable and disable times with active low output and pull-up load

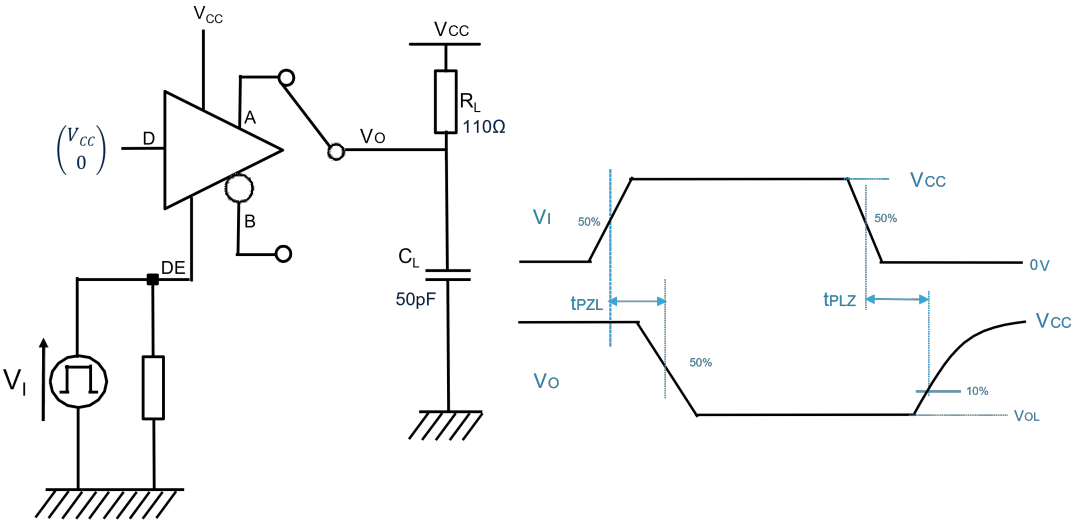


Figure 7. Receiver output rise and fall times and propagation delay

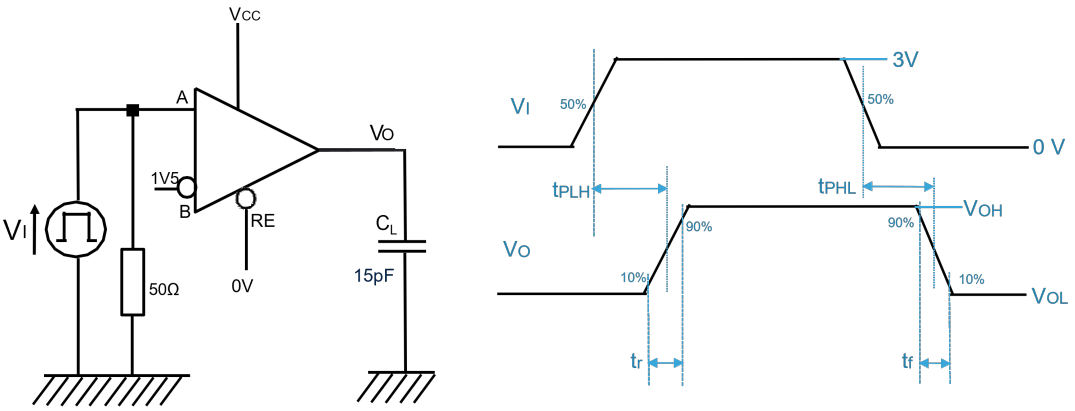


Figure 8. Receiver enable/disable times with driver enabled

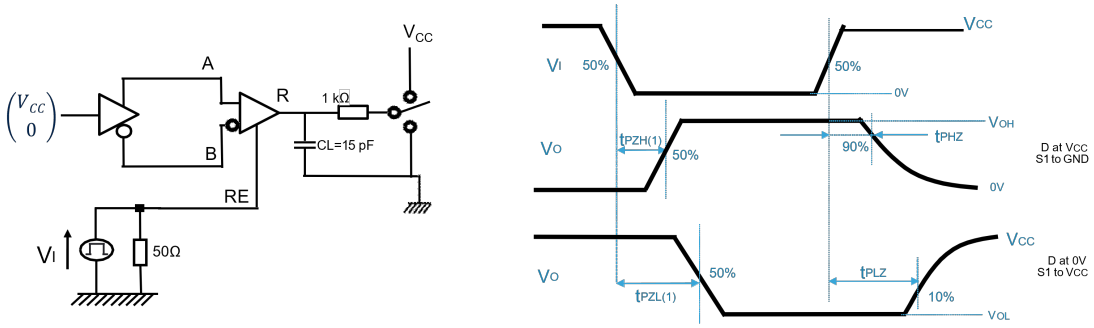


Figure 9. Receiver enable/disable times with driver disabled

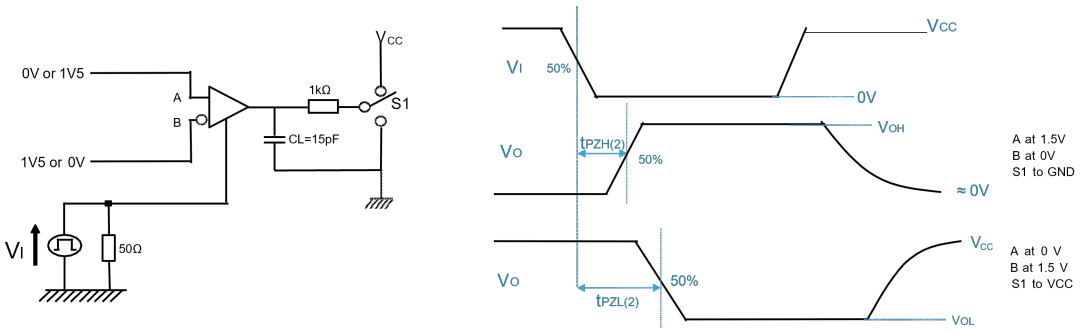
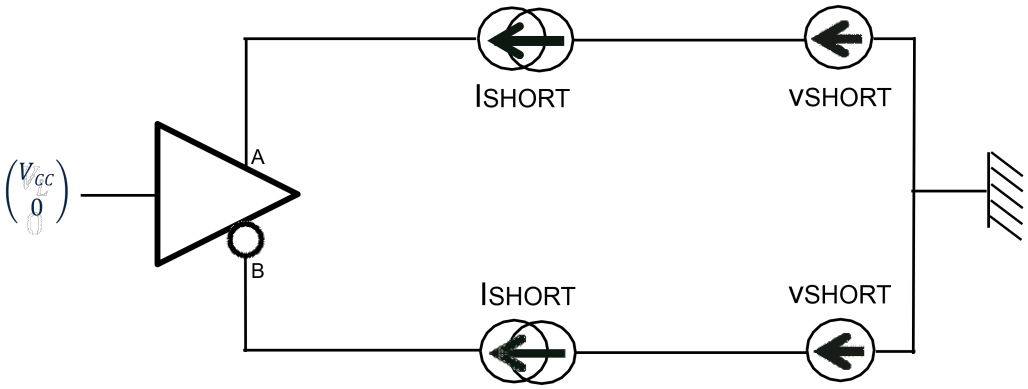
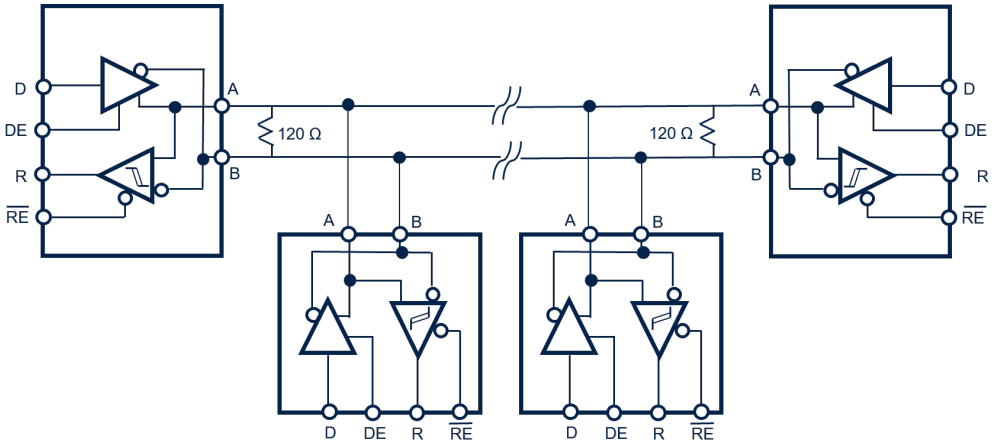


Figure 10. Short-circuit output current measurement



When one of the driver outputs is shorted to a voltage source (named V_{SHORT}) between -7 V to +12 V stabilized, the current does not exceed 250 mA and the driver is protected.

Figure 11. **Typical half-duplex RS485 network**



5 Typical characteristics - All devices

Figure 12. Driver output voltage vs. driver output current @ V_{CC} = 5 V

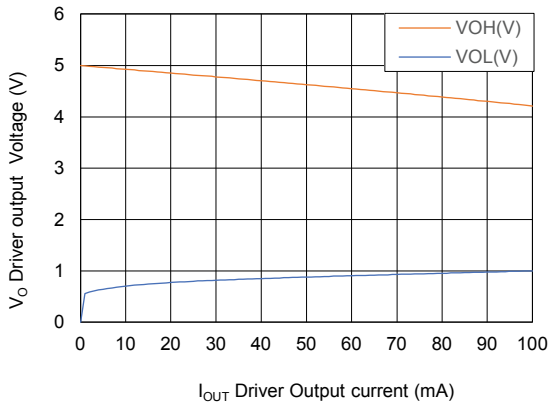


Figure 13. Driver differential output voltage vs. driver output current @ V_{CC} = 5 V

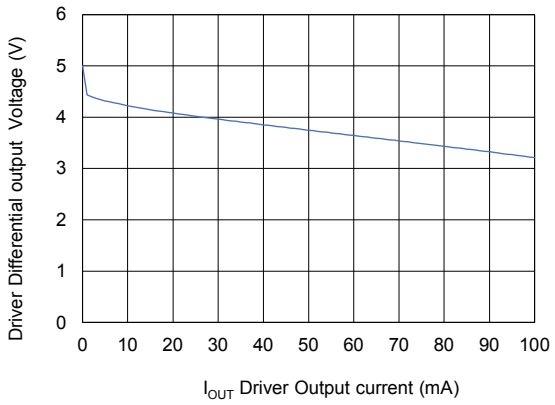


Figure 14. Receiver output vs. input @ V_{CC} = 5.5 V

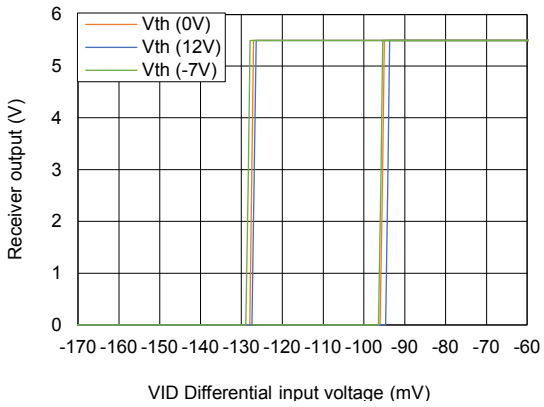


Figure 15. Driver output voltage vs. driver output current @ V_{CC} = 3.3 V

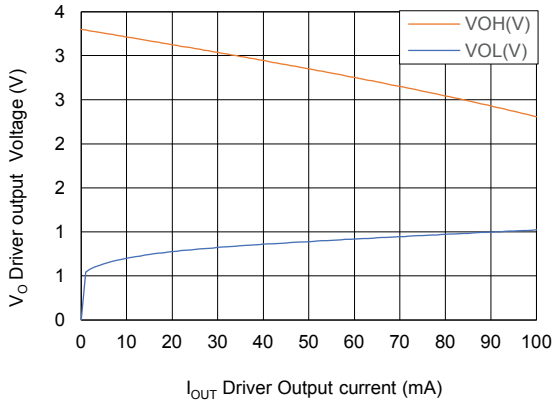


Figure 16. Driver differential output voltage vs. driver output current @ V_{CC} = 3.3 V

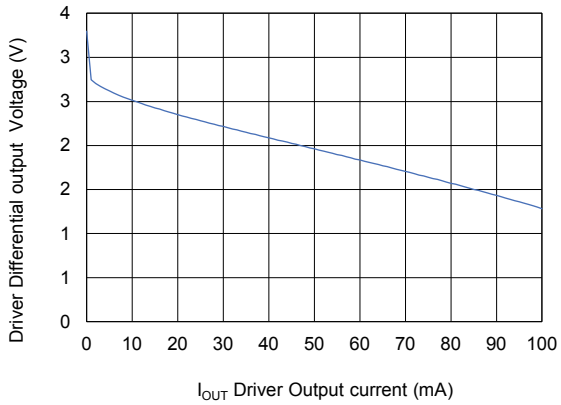


Figure 17. Receiver output vs. input @ V_{CC} = 3 V

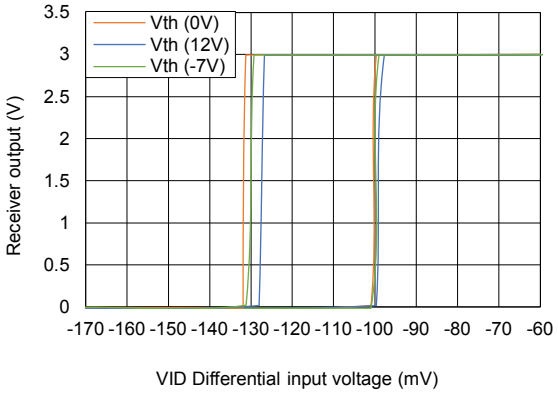


Figure 18. Driver output current vs. power supply with R_L=54Ω

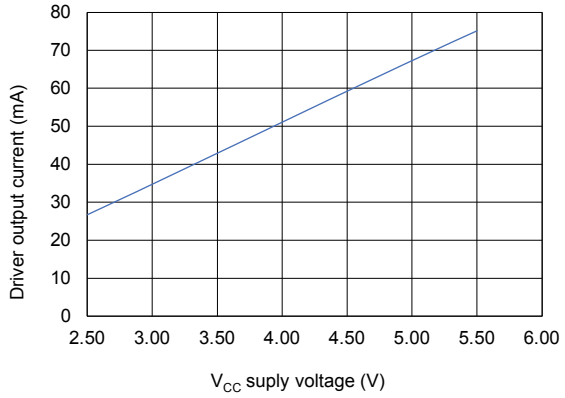
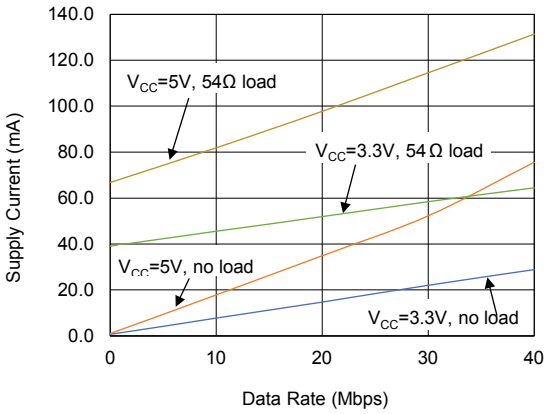


Figure 19. Supply current vs. data rate



5.1 Typical characteristics - ST4E1240 - SO8 package

Figure 20. Shutdown supply current vs. temperature, DE = GND, $\overline{RE}$ = V_{CC}, @ V_{CC} = 3.3 V and V_{CC} = 5 V

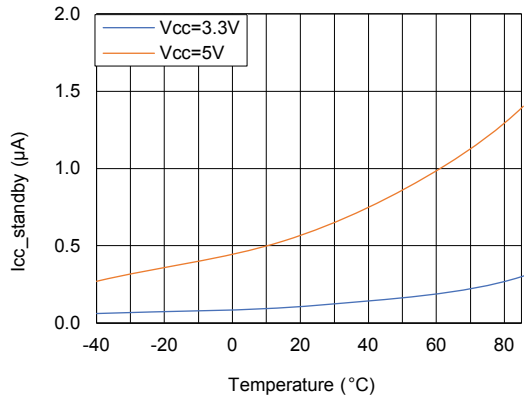


Figure 21. No-load supply current vs. temperature, DE = GND, $\overline{RE}$ = GND, @ V_{CC} = 3.3 V and V_{CC} = 5 V

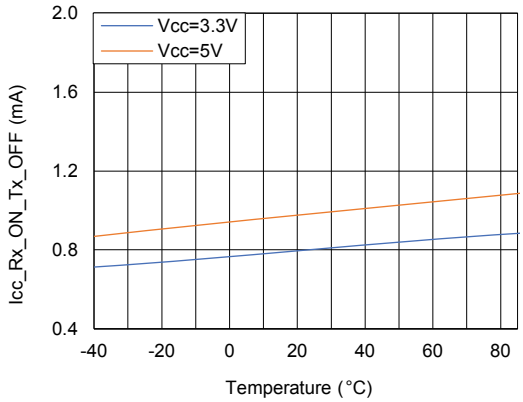


Figure 22. No-load supply current vs. temperature, DE = V_{CC}, $\overline{RE}$ = V_{CC}, @ V_{CC} = 3.3 and V_{CC} = 5 V

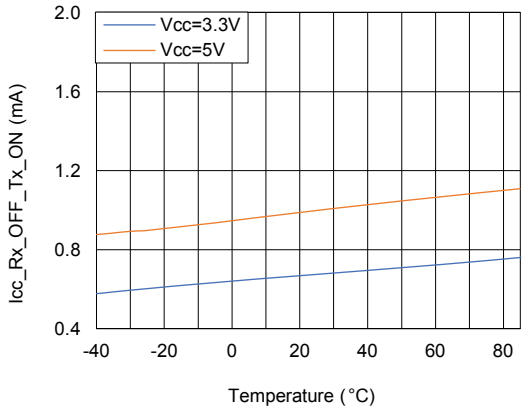


Figure 23. No-load supply current vs. temperature, DE = V_{CC}, $\overline{RE}$ = GND, @ V_{CC} = 3.3 V and V_{CC} = 5 V

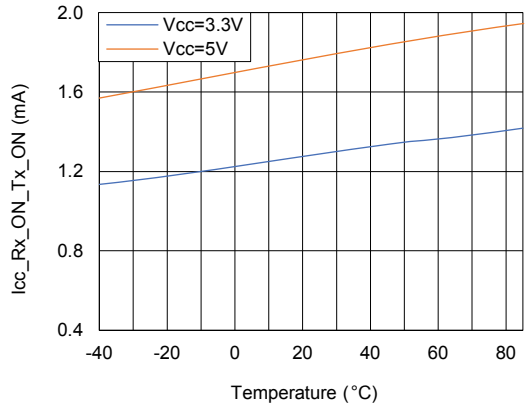


Figure 24. Differential driver output voltage vs. temperature

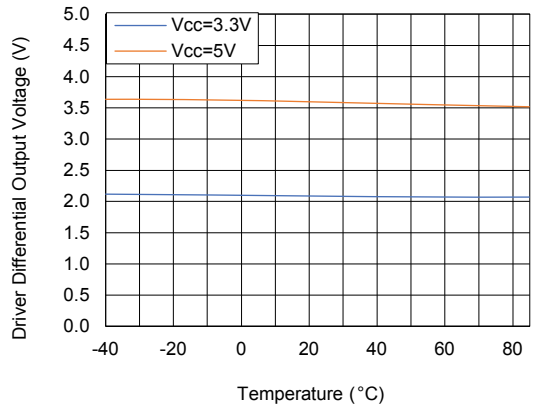


Figure 25. Driver rise and fall times vs. temperature @ V_{CC} = 5.5 V

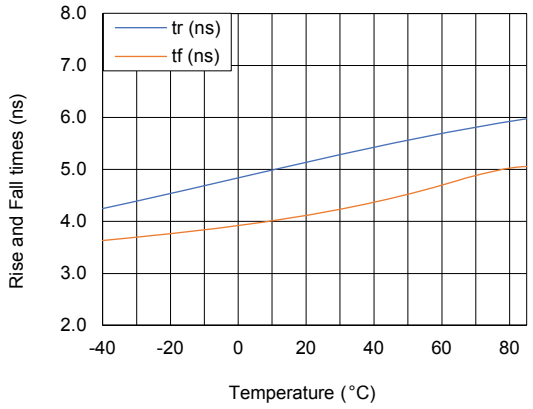


Figure 26. Driver propagation delay vs. temperature @ V_{CC} = 5.5 V

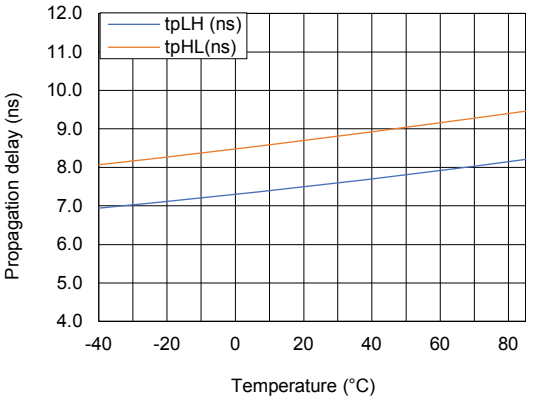


Figure 27. Driver rise and fall times vs. temperature @ V_{CC} = 3 V

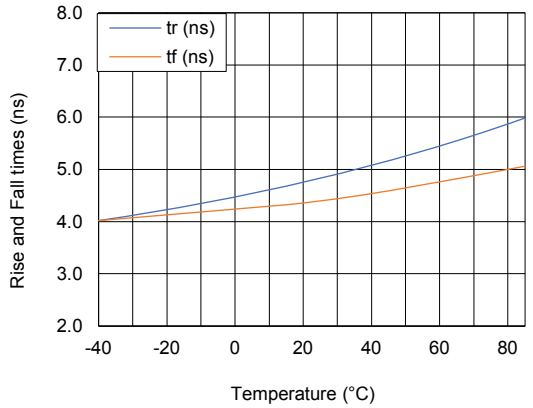


Figure 28. Driver propagation delay vs. temperature @ V_{CC} = 3 V

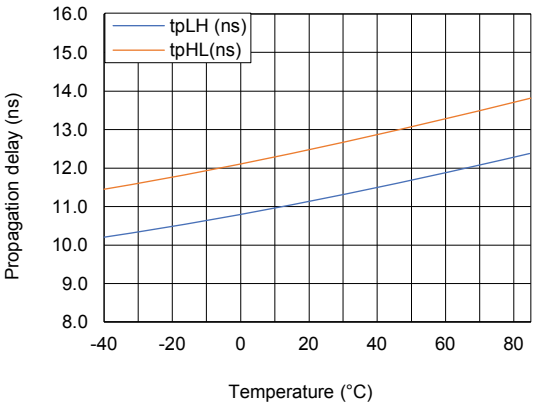


Figure 29. Receiver propagation delay vs. temperature, with C_L = 20 pF

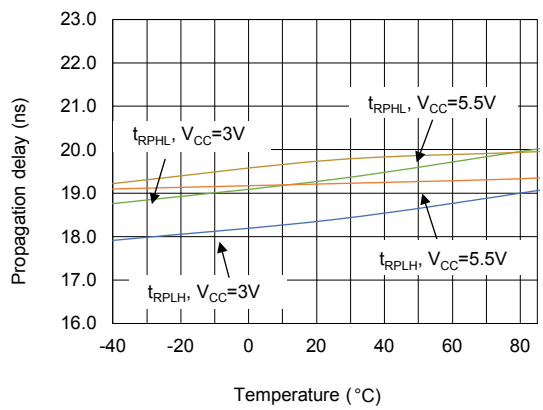


Figure 30. Eye diagram @ V_{CC} = 5 V, data rate 40 Mbps, d=0.1m

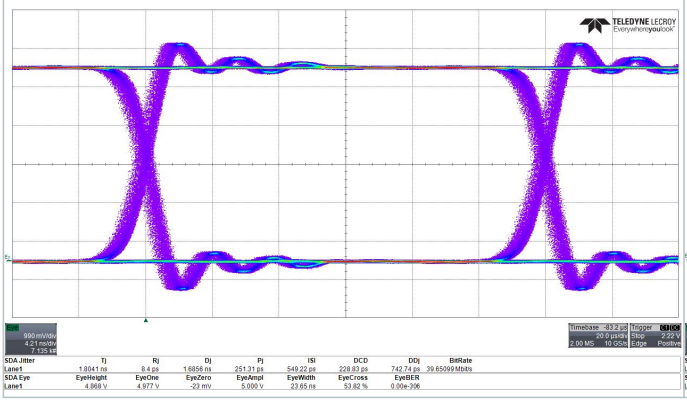
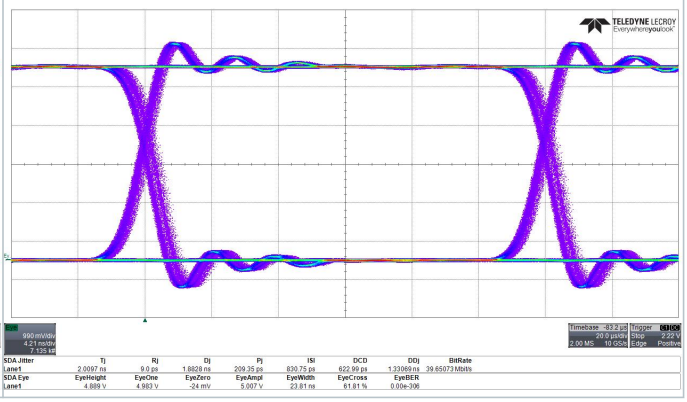


Figure 31. Eye diagram @ V_{CC} = 5 V, data rate 40 Mbps, d=3m



5.2 Typical characteristics - ST4E1216 and ST4E1240 - DFN8 package

Figure 32. Shutdown supply current vs. temperature, DE = GND, $\overline{RE}$ = V_{CC}, @ V_{CC} = 3.3 V and V_{CC} = 5 V

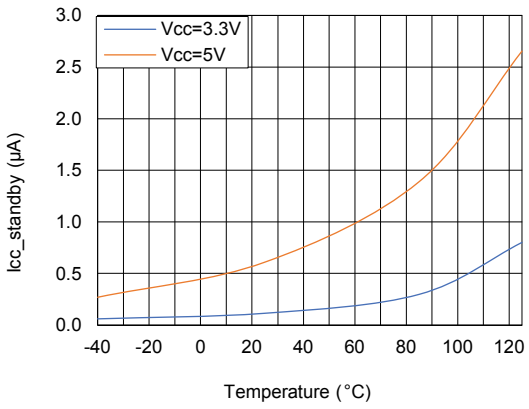


Figure 33. No-load supply current vs. temperature, DE = GND, $\overline{RE}$ = GND, @ V_{CC} = 3.3 V and V_{CC} = 5 V

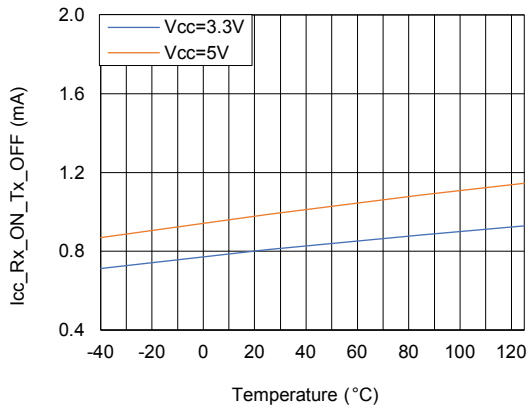


Figure 34. No-load supply current vs. temperature, DE = V_{CC}, $\overline{RE}$ = V_{CC}, @ V_{CC} = 3.3 and V_{CC} = 5 V

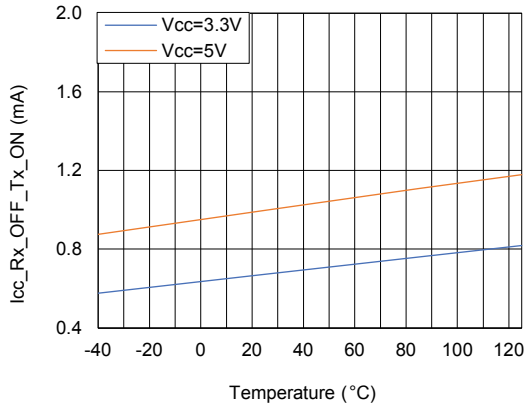


Figure 35. No-load supply current vs. temperature, DE = V_{CC}, $\overline{RE}$ = GND, @ V_{CC} = 3.3 V and V_{CC} = 5 V

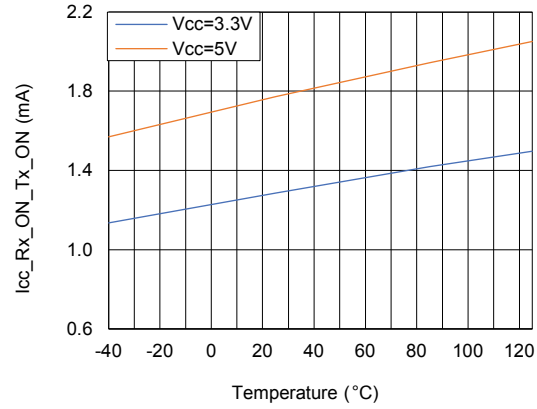


Figure 36. Differential driver output voltage vs. temperature

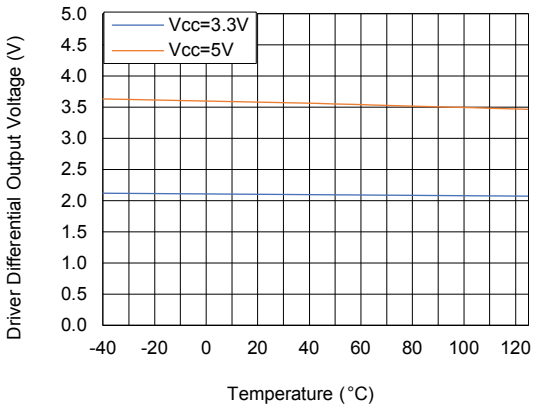


Figure 37. Driver rise and fall times vs. temperature @ V_{CC} = 5.5 V

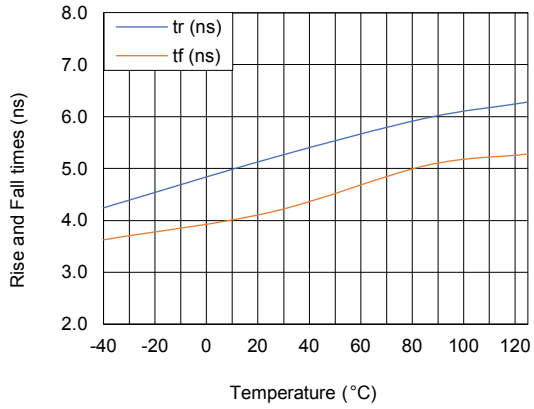


Figure 38. Driver propagation delay vs. temperature @ V_{CC} = 5.5 V

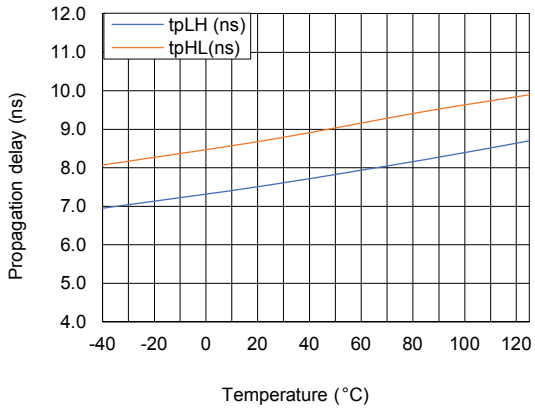


Figure 39. Driver rise and fall times vs. temperature @ V_{CC} = 3 V

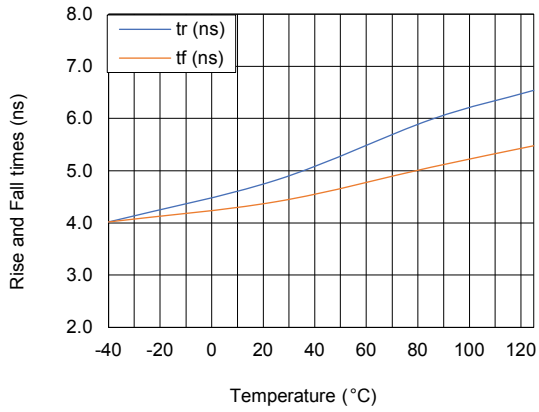


Figure 40. Driver propagation delay vs. temperature @ V_{CC} = 3 V

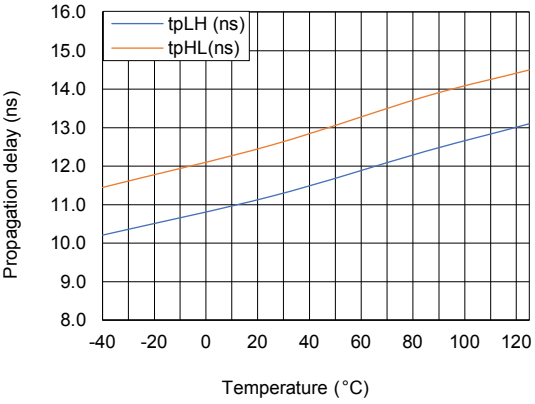


Figure 41. Receiver propagation delay vs. temperature, with C_L = 20 pF

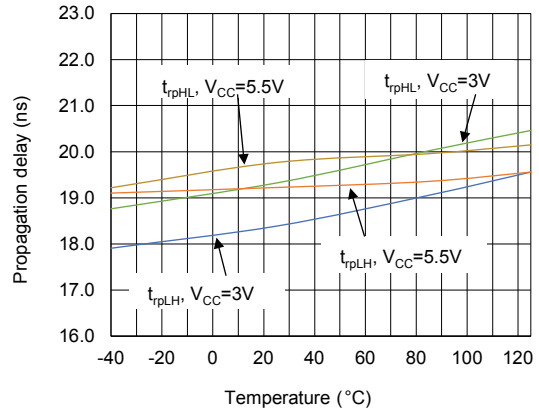


Figure 42. Eye diagram for the ST4E1216 @ V_{CC} = 5 V, data rate 16 Mbps, d = 3 m

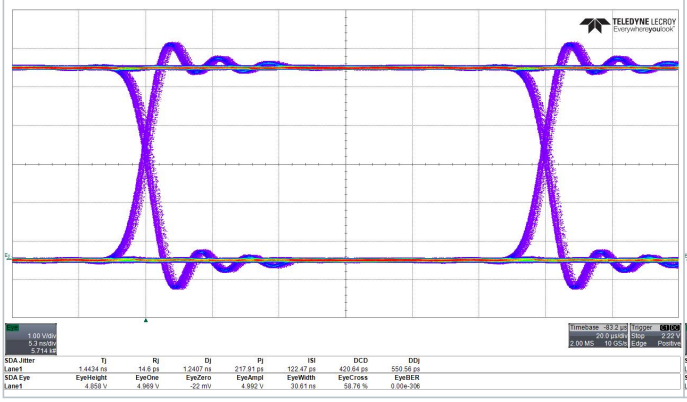
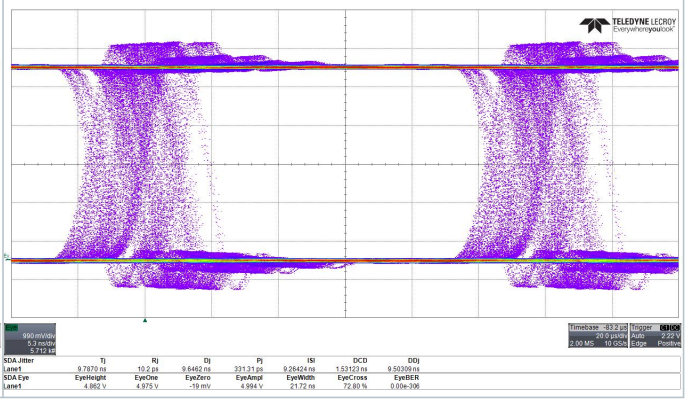


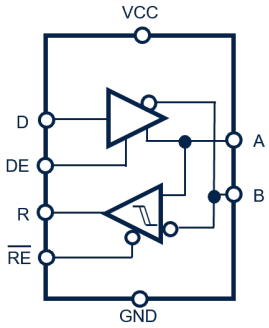
Figure 43. Eye diagram @ V_{CC} = 5 V, data rate 16 Mbps, d = 80 m



6 Detailed description

The ST4E1216 and ST4E1240 are a half-duplex differential RS-485 transceiver, suitable for data transmission up to 40 Mbps. The devices support 64 bus nodes minimum. The receiver and driver are activated through the dedicated pins DE and $\overline{RE}$. Its functional block diagram is shown below.

Figure 44. Block diagram



Device functional modes

The various functional modes of the ST4E1216 and ST4E1240 are detailed in the following function tables.

When the driver enable pin DE is high, the driver is enabled. The differential signal $V_{OD} = V_A - V_B$ follows the logic state of the signal present on input D, that is V_{OD} is positive if D is high, V_{OD} is negative when D is low.

When DE logic is low, A and B are set to high impedance, the driver is disabled, and the D signal does not impact the outputs. The DE pin has an internal pull-down resistor to the ground, which disables the driver by default if left open.

The D pin has an internal pull-up resistor to V_{CC}, thus when left open while the driver is enabled, output A is high and B low by default.

Table 11. Driver truth table

INPUT D	ENABLE DE	OUTPUT A	OUTPUT B	Function
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	Open	Z	Z	Driver disabled by default
Open	H	H	L	Actively drive bus high by default

When the receiver enable pin $\overline{RE}$ is logic low, the receiver is enabled. When the differential input voltage $V_{ID} = V_A - V_B$ is higher than the positive input threshold V_{TH+}, the receiver output R turns high. When V_{ID} is below the negative threshold V_{TH-}, the output R turns low. And when V_{ID} is in-between both threshold voltages, R is indeterminate.

If $\overline{RE}$ is logic high, R is high impedance and the V_{ID} polarity and voltage do not impact it. The $\overline{RE}$ pin has an internal pull-up resistor, thus when left open, the receiver output is disabled by default.

The ST4E1216 and ST4E1240 architecture turns receiver output in a fail-safe high state when the transceiver is disconnected from the bus (open), the bus lines A, B are shorted together (short), or the bus is not actively driven (idle).

Table 12. **Receiver truth table**

Differential input $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R	Function
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	I	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	Open	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

Shutdown mode

Shutdown mode is initiated when driving DE low and $\overline{RE}$ high. In this state, the device draws less than 3.5 µA of current in all temperature and power supply conditions. Shutdown mode is entered in typically 2 µs at V_{CC} 5 V and ambient temperature of 25 °C.

The ST4E1216 and ST4E1240 are designed for bidirectional data communications on multipoint bus transmission lines. Figure 11 shows a typical network application circuit. To minimize reflections, the line should be terminated at both ends with its characteristic impedance and stub lengths to be kept as short as possible from the main line.

Fail-safe receiver

The ST4E1216 and ST4E1240 have a fail-safe receiver to ensure a logic level on the bus and prevent any indeterminate state. The following conditions can be detected.

- Open bus such as a disconnected connector
- A shorted bus such as a damaged cable creating a short of the twisted pair
- An idle bus that occurs when no device on the bus is actively driving

In any of these cases, the differential receiver drives a fail-safe logic high level so that the output of the receiver is not indeterminate.

Hot-swap capability

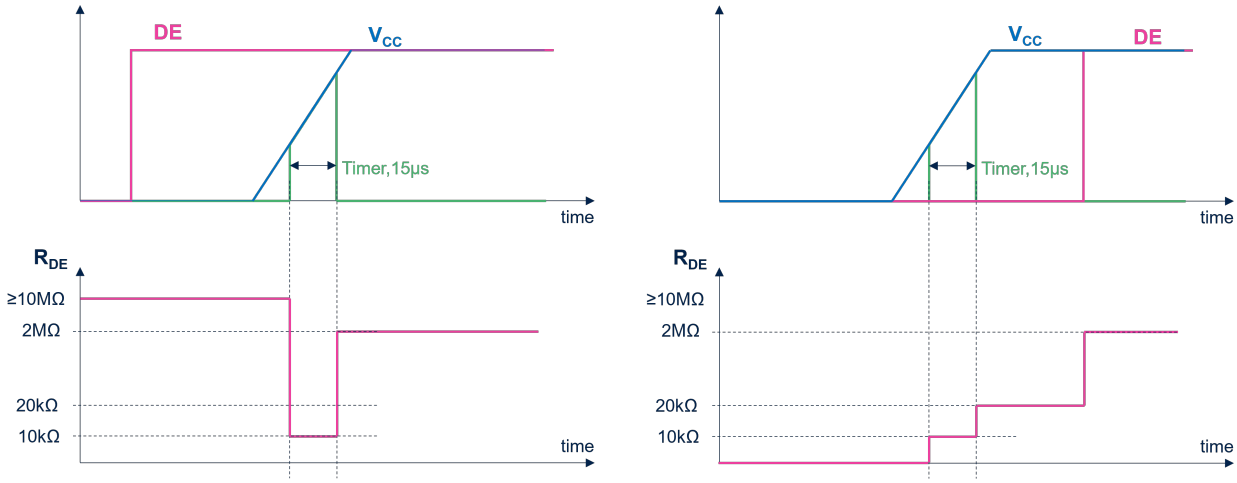
The enable pins DE and $\overline{RE}$ are critical pins during a switch-on or plug-in phase on the RS485 bus. To prevent these pins from driving into unwanted states on the bus due to possible disturbances during these steps, the ST4E1216 and ST4E1240 features an integrated hot-swap structure to avoid these potential problems.

Assuming a parasitic capacitance may be present on the board between the nodes DE and GND, or $\overline{RE}$ and V_{CC}; when the power supply rises, the MCU may drive an undetermined state on the nodes DE and $\overline{RE}$. Depending on the input impedance on nodes DE and $\overline{RE}$, it can generate an unwanted signal on bus pins A, B.

A parasitic capacitance up to 100 pF is efficiently discharged with the hot-swap structure of the ST4E1216 and ST4E1240.

The new ST RS485 transceivers manage dynamically the input impedance on DE and $\overline{RE}$ versus V_{CC}. A typical transient resistor of 6 kΩ is seen during the rising edge of the power supply, during a defined time of 15 µs typically. This allows fast discharge of parasitic capacitance, preventing any unwanted signal on the bus pins. A second typical transient resistor of 20 kΩ is still present until the V_{CC} supply is fully established. Then, the 2 MΩ resistors are the connected pull-up or pull-down resistor on both DE and $\overline{RE}$ terminals during normal ON operation for current consumption considerations. An example is shown below for the impedance management on the DE terminal. Such a structure is also present on $\overline{RE}$ versus V_{CC}.

Figure 45. **Hot-swap management with DE rising high before and after V_{CC}**



Electrostatic discharge (ESD) protection

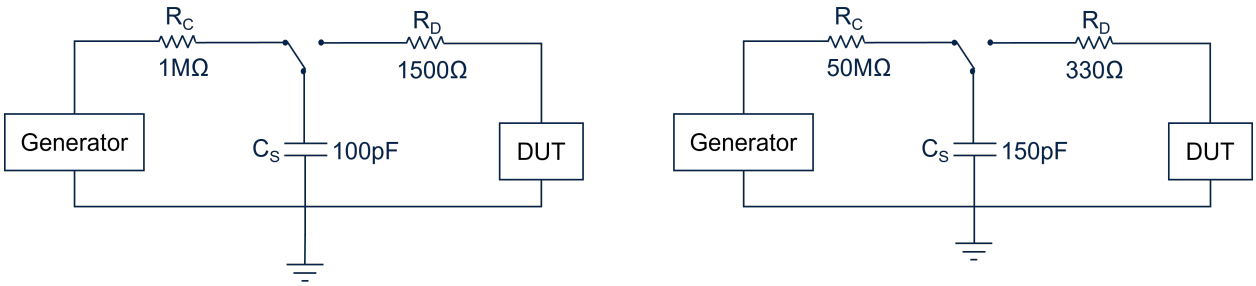
The ST4E1216 and ST4E1240 have internal protection against electrostatic discharge (ESD).

At circuit level, the ST4E1216 and ST4E1240 comply with the human body model (ANSI/ESDA/JEDEC JS-001) to guarantee robustness during the manufacturing process. All the pins of the ST4E1216 and ST4E1240 sustain 2 kV.

Because these transceivers are part of a system and can be connected to its outside through the bus terminals A and B, an ESD protection is implemented on A and B to comply with IEC 61000-4-2 standard.

The schematic below compares the simplified pulse generator between the circuit-level ESD pulse and the system-level ESD pulse.

Figure 46. **HBM JEDEC (left) and IEC61000-4-2 (right) generator simplified schematics**

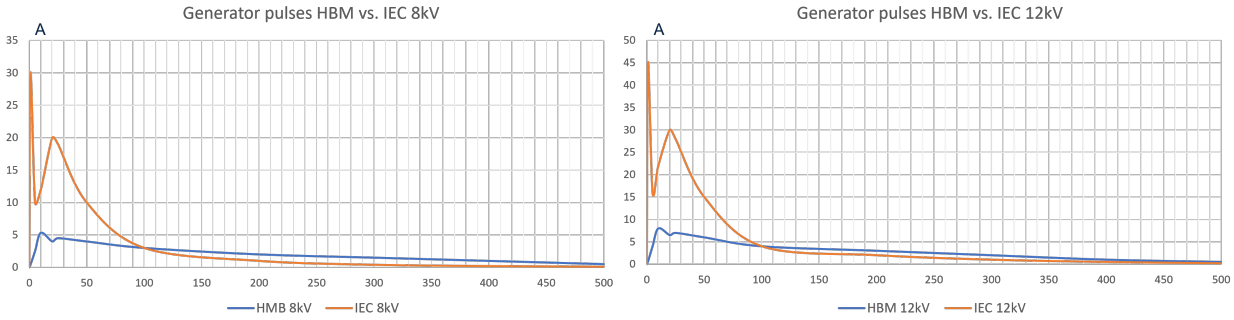


Peak current 0.7 A*kV
Rise time of pulse: 2 ns to 10 ns

Peak current 3.75 A*kV
Rise time of pulse: 0.6 ns to 1 ns

For an equivalent ESD pulse voltage, the peak current and rise time of the pulse is much higher for the IEC61000-4-2 than for the HBM. This can be shown by the pulse's diagrams below, for 8 kV and 12 kV respectively.

Figure 47. HBM JEDEC and IEC61000-4-2 waveforms comparison



The IEC61000-4-2 standard is more severe than the HBM ESD test and significantly increases the robustness of the equipment. IEC61000-4-2 8 kV protections are commonly implemented.

The ST4E1216 and ST4E1240 furthermore increase the robustness of systems thanks to the dedicated IEC61000-4-2 12 kV protections on bus terminals A and B. There are two methods of ESD testing: contact discharge and air discharge. In the contact discharge method, the electrode of the test generator is held in contact with an exposed conductor on the equipment under test (EUT). In the air discharge, the electrode of the generator is moved from a distance towards the EUT until an arc occurs. The contact discharge offers the best reproducibility and is chosen to be the test method for IEC61000-4-2.

The ST4E1216 and ST4E1240 comply with IEC61000-4-2 12 kV contact discharge.

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SO8 package information

Figure 48. SO8 package outline

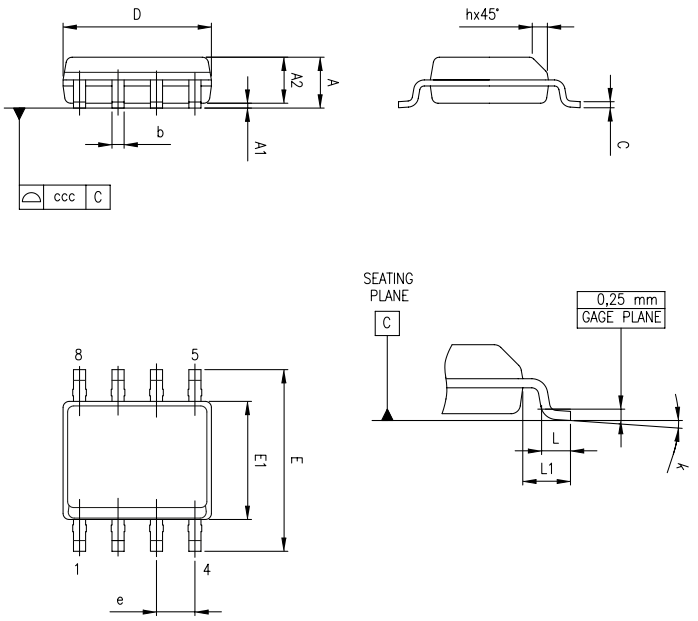
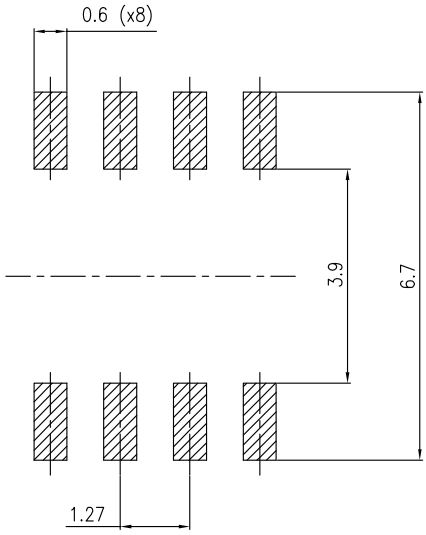


Table 13. SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.04		0.010
A2	1.25			0.049		
b	0.28	0.40	0.48	0.011	0.016	0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40	0.635	1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004

Figure 49. **SO8 recommended footprint (mm)**



7.2 DFN8 3x3 package information

Figure 50. **DFN8 3x3 package outline**

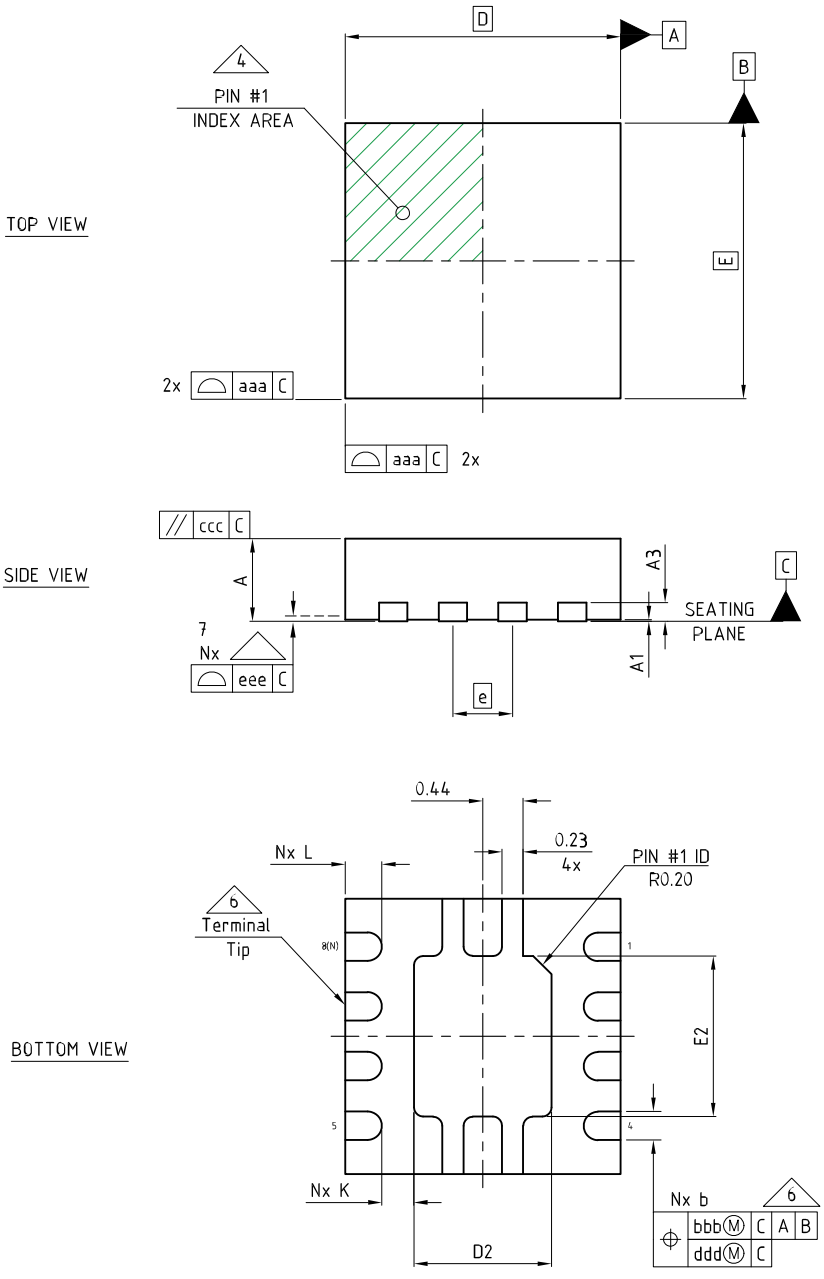
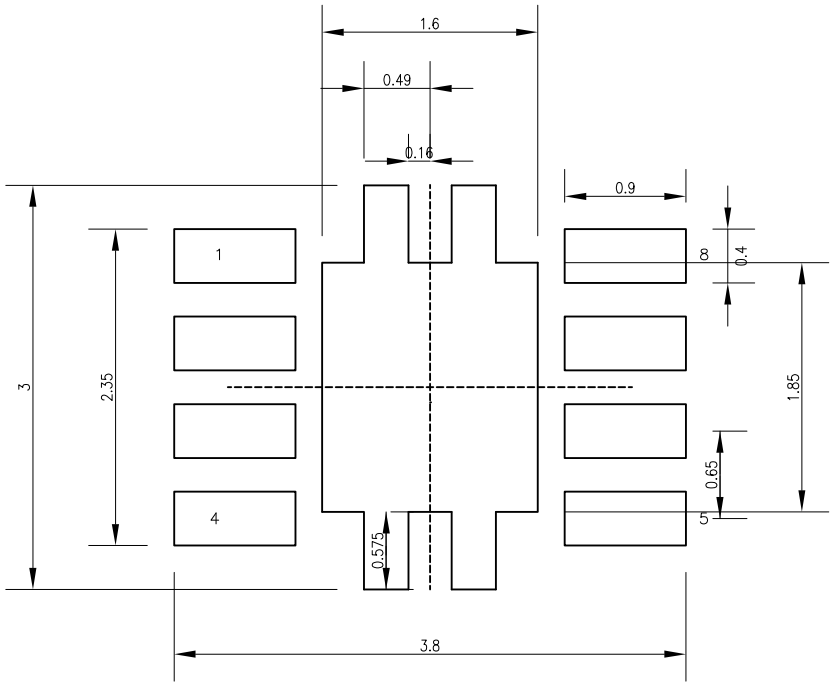


Table 14. **DFN8 3x3 mechanical data**

Ref.	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.26	0.31	0.36
D		3 BSC	
E		3 BSC	
e		0.65 BSC	
D2	1.45	1.50	1.55
E2	1.70	1.75	1.80
K	0.20	-	-
L	0.30	0.40	0.50
N		8	
Ne		4	
		TOLERANCE	
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Figure 51. **DFN8 3x3 recommended footprint**



8 Ordering information

Table 15. **Order code**

Order code	Temperature range	Package	Marking
ST4E1216IDT	-40 °C to +125 °C	SO-8	T4E1216I
ST4E1240DT	-40 °C to +85 °C		T4E1240
ST4E1240IQT	-40 °C to +125 °C	DFN8	240I

Revision history

Table 16. **Document revision history**

Date	Revision	Changes
09-Jan-2024	1	Initial release.
12-Feb-2024	2	Added new part number ST4E1216. Updated features and description on the cover page, Figure 1 and Table 14. Order code.
06-Nov-2024	3	Added new package DFN8 3 x 3 and Section 7.2. Updated figure, features and device summary on the cover page, Figure 1, Table 3 and Table 15.

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